LISTING OF THE CLAIMS

1. (Original) A processor, comprising:

an instruction pipeline for executing processor instructions wherein said processor instructions define a memory access size; and

a cache memory for storing cache lines in a plurality of memory banks that have a block size that is greater than said memory access size, said cache memory including mapping logic for storing contiguous groups of bits, of size equal to said memory access size, in different ones of said plurality of memory banks.

2. (Original) The processor of claim 1, wherein said instruction pipeline comprises:

a plurality of functional units for executing said processor instructions.

3. (Original) The processor of claim 2 wherein said plurality of functional units are operable to initiate a memory access to a first memory address of data stored in said cache memory during pipeline execution of a first processor instruction while memory access to a second memory address that is immediately before said first memory address is occurring during pipeline execution of a second processor instruction.

4. (Original) The processor of claim 3 wherein said first processor instruction is obtained by an instruction fetch unit while said second processor instruction is being processed in said instruction pipeline.

5. (Original) The processor of claim 1 wherein said cache memory obtains cache lines from main memory.

6. (Original) The processor of claim 1 wherein said cache memory obtains cache lines from a lower level cache.

7. (Original) The processor of claim 1 wherein said mapping logic stores adjacent words in said cache lines in different ones of said plurality of memory banks.

8. (Original) A method for operating a processor, comprising:

executing instructions in an instruction pipeline, wherein said instructions define a memory access size;

storing cache lines in memory banks of cache memory included in said processor, said memory banks having a block size that is greater than said memory access size, wherein said storing causes contiguous groups of bits, of size equal to said memory access size, to be stored in different ones of said memory banks.

9. (Original) The method of claim 8 wherein said executing instruction in said instruction pipeline includes:

executing instructions in a plurality of functional units in parallel.

10. (Original) The method of claim 8 further including:

initiating a first memory access to a first memory address of data stored in said cache memory during pipeline execution of a first instruction; and

initiating a second memory access to a second memory address of data stored in said cache memory during pipeline execution of a second instruction while said first memory access is pending, wherein said second memory address is immediately after said first memory address by a number of bits equal to said memory access size.

11. (Original) The method of claim 10 further comprising:

fetching said second instruction while said first memory access is pending.

12. (Original) The method of claim 8 further comprising:

retrieving cache lines from main memory; and

storing said cache lines in said cache memory.

13. (Original) The method of claim 8 further comprising:

retrieving cache lines from a lower level cache; and

storing said cache lines in said cache memory.

14. (Original) The method of claim 8 wherein said storing stores adjacent words in said cache lines in different ones of said memory banks.

15. (Original) A processor, comprising:

a pipeline means for executing processor instructions wherein said processor instructions define a memory access size; and

a cache memory means for storing cache lines in memory banks according to a block size that is greater than said memory access size, wherein said cache memory means stores contiguous groups of bits, of size equal to said memory access size, in different ones of said plurality of memory banks.

16. (Original) The processor of claim 15 wherein said pipeline means includes:

a plurality of functional units for executing said processor instructions in parallel.

17. (Original) The processor of claim 16 wherein said plurality of functional units are operable to initiate a memory access to a first memory address of data stored in said cache memory means during pipeline execution of a first processor instruction while memory access to a second memory address that is immediately before said first memory address is occurring during pipeline execution of a second processor instruction.

18. (Original) The processor of claim 17 further comprising:

an instruction fetch means for fetching said first and second processor instructions, wherein said instruction fetch means fetches said first processor instruction while said second memory access is occurring.

19. (Original) The processor of claim 15 wherein said cache memory means retrieves said cache lines from main memory.

20. (Original) The processor of claim 15 wherein said cache memory means stores adjacent words of said cache lines in different ones of said memory banks.